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<i>DB=TDBD; PLUR=YES; OP=OR</i>		
<u>L18</u> L17	0	<u>L18</u>
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<u>L13</u> L9 and source and drain	84	<u>L13</u>
<u>L12</u> L11	123	<u>L12</u>
<u>L11</u> L8	123	<u>L11</u>
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<u>L9</u> L8	123	<u>L9</u>
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<u>L7</u> L1 and transistor and SiC	300	<u>L7</u>
<u>L6</u> L1 and transistor and SiC5	0	<u>L6</u>
<u>L5</u> L4 and SiC	0	<u>L5</u>
<u>L4</u> L1 and l2	0	<u>L4</u>
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<u>L1</u> drift	47633	<u>L1</u>

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